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MID TERM EXAMINATIONS – July 2024

Programme	:	**B.Tech.**	Semester	:	**Fall Semester 2024-2025**
Course Title	:	**Digital Logic and Computer Architecture**	Course Code	:	**CSA2003**
Date/Session	:	**15 July 2024/ Session I**	Slot	:	**B12+B13+E11+E12+E13**
Time	:	**1 ½ hours**	Max. Marks	:	**50**

Answer all the Questions

Q.No.	Sub. Sec.	Question Description	Marks
1	(a)	Perform the following operations using 2's complement method using 8-bit representation for each number: (i) 48-23 (ii) 23-48 (iii)48-(-23) (iv)-48-23	6
	(b)	Convert the hexadecimal number CA5E to following number systems: (i) Decimal (ii) Octal	4
2		Simplify the following logic function using K-map method: $f(A,B,C,D) = AB\bar{C}D + \bar{A}BCD + \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{D} + A\bar{C} + A\bar{B}C + \bar{B}$	10
3		Discuss the necessity and functioning of a master-slave flip-flop in digital circuits. Use the D flip-flop as an example to illustrate your explanation containing the truth table and timing diagram.	10
4		Provide a comparative analysis covering definitions, structural and operational differences, and applications of multiplexers and de-multiplexers. Use diagrams and truth tables to illustrate your points.	10
5		Design 2-bit Up and Down ripple counters using suitable flip-flops.	10

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