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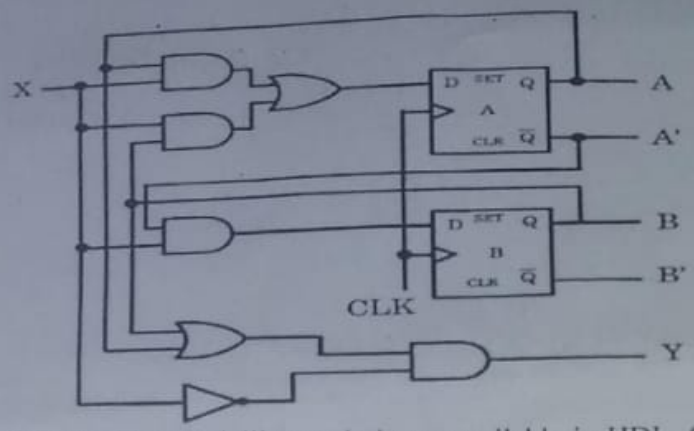
TERM END EXAMINATIONS (TEE) – May 2024

Programme	:	BCE	Semester	:	Winter Semester 2023-24
Course Title/ Course Code	:	Digital Logic Design/ ECE2002	Slot	:	B11+B12+B13
Time	:	3 Hrs.	Max. Marks	:	100

Answer ALL the Questions

Q. No.		Question Description	Marks
		PART A – (60 Marks)	
1	(a)	(i) Convert $(FACE)_{16}$ into its binary, octal, and decimal equivalent.	9
		(ii) Convert 23.625_{10} to octal equivalent.	3
		OR	
	(b)	(i) Simplify and implementation the following SOP function using NOR gates, F (A, B, C, D) = ∑m (0,1,4,5,10,11,14,15)	6
		(ii) Design the circuit by Using NAND gates F= ABC'+ DE+ AB'D'	6
2	(a)	Describe a 4-bit Binary to gray code converter and implement it using logic gates	12
		OR	
	(b)	Implement the following Boolean function using an 8:1 Multiplexer and also using 4:1 Multiplexer F (w, x, y, z) =∑m (1, 2, 3, 6, 7, 8, 11, 12, 14).	12
3	(a)	Analyze the circuit of a JK flip flop and realize JK flip flop using D flip flop.	12
		OR	
	(b)	A sequential circuit with two D flip flops A and B, input X and output Y is specified by the following next state and output equations: A (t+1) = AX+BX; B (t+1) = A'X; Y= (A+B) X'. (i) Draw the logic diagram. (ii) Construct the state table. (iii) Draw the state diagram.	12
4	(a)	Consider the design of 4-bit synchronous BCD counter that counts in the following way using JK flipflop. 0000,0001,0010, 0011…..,1001 and back to 0000 (i) Draw the state diagram (ii) List the next state table (iii)Draw the logic diagram of the circuit	12
		OR	
	(b)	Analyze the following clocked sequential circuit and obtain the state equations and state diagram.	12



5 (a) Describe the modelling techniques available in HDL. Give the Verilog HDL code to realize a full adder using gate level modelling 12

OR

(b) Write the Verilog HDL code for 4 bit Binary UP/DOWN counter using JK flip flops 12

PART B – (40 Marks)

6 Simplify the following Boolean expression AC'+B'D+A'CD+ABCD in (i) sum of product (ii) product of sum using K-map. 8

7 Realize 4 x 16 decoder using two 3 x 8 decoders with enable input. 8

8 Analyze SISO and PIPO shift registers with neat logic diagram and sample data inputs. 8

9 What is the difference between ring and Johnson counter? Draw the circuit of four-bit Johnson counter and explain its working. Draw the timing diagram of a 4-bit Johnson counter 8

10 Create a Verilog HDL module listing for an 8:1 MUX that is based on the assign statement. Use a 3-bit select word (S2, S1, and S0) to map the selected input Pi (i=0, 1....7) to the output. 8

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