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TERM END EXAMINATIONS (TEE) – August 2024

Programme	:	**B.Tech.**	**Semester**	:	**Fall Semester 2024-2025**
Course Name	:	**Digital Logic Design**	**Course Code**	:	**ECE2002**
Date/Session	:	**21 Aug 2024/Session I**	**Slot**	:	**A14+B14+C14+E14+F14**
Time	:	**3 Hrs.**	**Max. Marks**	:	**100**

Answer ALL the Questions

Q. No.		Question Description	Marks
		PART A – (60 Marks)	
1	(a)	$A = (10)_{10}$ and $B = (12)_{10}$ Perform the binary operations: A+B, A-B, B-A and AxB (multiply). Verify the answers. Use 2's complement method for subtraction.	12
		OR	
	(b)	Simplify and minimize the function O using Boolean algebra. $$O = \overline{(A + BC)(\bar{A}\bar{B} + \bar{C})}$$ Draw the reduced circuit using basic gates.	12
2	(a)	Draw 4-bit binary adder-subtractor (combined). Explanation not required. Show the addition and subtraction of A = 1001 and B = 1000 using the adder-subtractor and verify the answers.	12
		OR	
	(b)	Design a combinational circuit with 4 binary inputs such that the output is 1 only when the input number (converted from binary to decimal) is divisible by 3.	12
3	(a)	Analyse the circuit given in Fig. 3 by writing its equations, state diagram and state table. (Ignore the pin R connected to reset)	12

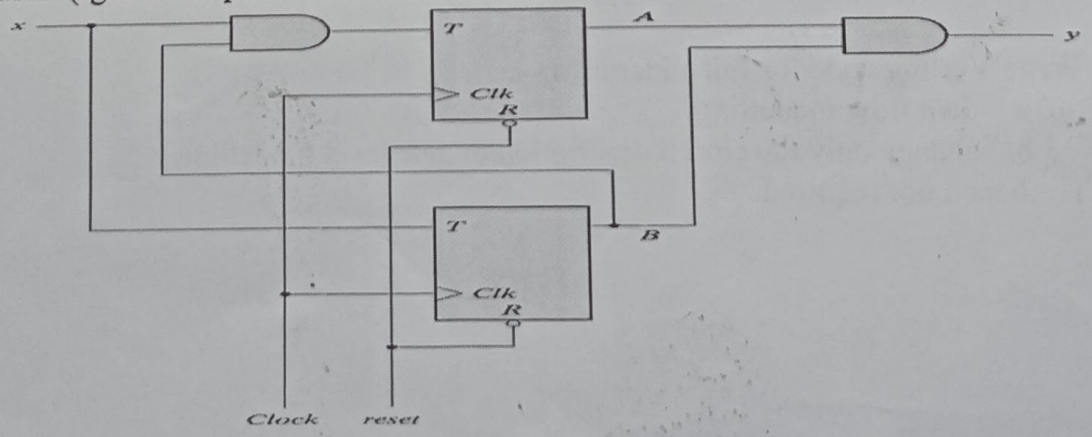

Fig. 3

OR

(b) Derive the characteristic equations of D, JK and T flipflops. 12

4 (a) Design a circuit that detects a sequence of three or more consecutive 0's in a string of bits coming through an input line. Use D-flipflops for the design. Is this Mealy machine or Moore machine? 12

OR

(b) Design a synchronous MOD-7 up counter. Explain the designing and draw the final state diagram and circuit. 12

5 (a) Write the Verilog code for testbench of a full adder module. (You may combine this with your answer to Q.10) 12

OR

(b) Write the behavioural Verilog code for a positive edge triggered D flipflop. The input D is connected directly to an external input x. Testbench is not required. 12

PART B – (40 Marks)

6 Convert $(100)_{10}$ to binary, octal, hex and BCD. 8

7 Implement the function $F(A,B,C,D) = ABD' + BC'D + CD$ using a multiplexer with 3 select lines. 8

8 Draw the output waveform (Q) for Fig. 8. JK flipflop is negative clock edge triggered. 8

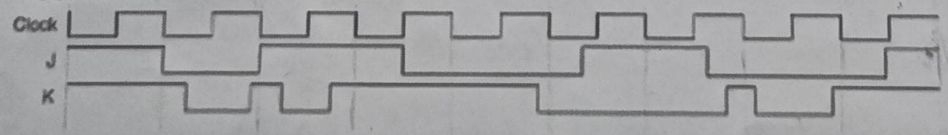

Fig. 8

9 Draw the block diagram of a 4-bit SIPO register. What will be output of the register after 4 clock cycles if a serial input of 1011010 is provided (starting with left most one)? Draw the waveforms. 8

10 Write Verilog code for full adder using
a. data flow modelling
b. change only the circuit description to gate level modelling.
Testbench not required. 8

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